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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,336	08/27/2003	Ching-Huei Wu	WUCH3033/EM	5344

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EXAMINER	
WON, BUMSUK	

ART UNIT	PAPER NUMBER
2879	

DATE MAILED: 11/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,336	WU ET AL.	
	Examiner	Art Unit	
	Bumsuk Won	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The amendment filed on 9/6/2006 has been entered.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-25 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Regarding the independent claims 1 and 10, the newly added claim limitation, "plurality of second electrodes alternate between connecting to" was never disclosed in the specification. In remarks filed on 9/7/2006, the Applicant states that the new claim limitation is supported throughout the specification as originally filed including figure 6 as described in figure 1. However, figure 1 does not show second electrodes being connected to conducting lines, and figure 6 only shows one set of conducting lines. Claims 2-9 and 11-25 are rejected due to claim dependency.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 10, 16, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (2003/0193792) in view of Yonekura (2002/0149313).

Regarding claim 1, Chang discloses a panel for an organic electroluminescent device (figs 5A-5C) comprising:

a substrate (501) having a first conducting area (left portion), a second conducting area (right portion), a third conducting area (bottom portion), and an active area (508);

wherein the active area locates between the first conducting area and the second conducting area; the third conducting area locates at one side of the active area; the first conducting area, the second conducting area, the third conducting area and the active area are integrated together on the surface of the substrate; and the third conducting area locates adjacent to the first conducting area, the second conducting area, and the active area;

first conducting lines (506) located in the first conducting area on the substrate;

second conducting lines (507) located in the second conducting area on the substrate;

third conducting lines (bottom portion of 506 and 507) located in the third conducting area on the substrate;

first electrodes (503) located in the active area, wherein the first electrode connects a third conducting line;

second electrodes (505) located in the active area, wherein the second electrode connects a first conducting line or a second conducting line; and

organic electroluminescent medium (fig 1C, 106) located in the active area, wherein the organic electroluminescent medium is sandwiched between the first electrode (104) and the second electrode (105);

wherein the first conducting line connects a third conducting line (506), the second conducting line connects a third connecting line (507), the first electrodes do not directly connect the second electrodes (506 not connected to 507), and the first conducting lines, the second conducting lines, the third conducting lines and the first electrodes are on the surface of the substrate (501).

Chang does not disclose the plurality of second electrodes alternate between connecting to a first and a second conducting line.

Yonekura discloses a panel (61) for an organic EL device (fig 9) having a plurality of first electrodes (67) and a plurality of second electrodes (70), and the second electrodes alternate between connecting to a first conducting line (64) and a second conducting line (65), for the purpose of distributing electric current in a balanced manner.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have second electrodes being alternated between connecting a first conducting line and a second conducting line disclosed by Yonekura in the panel disclosed by Chang, for the purpose of distributing electric current in a balanced manner.

Regarding claim 2, Chang discloses bonding unit (502) located in the third conducing area for bonding a cable (fig 3, 306). The reason for combining is same as claim 1.

Regarding claim 3, the examiner notes that the claim limitation the cable being bonded through COG sealing is drawn to a process of manufacturing which is incidental to the claimed

apparatus. It is well established that a claimed apparatus cannot be distinguished over the prior art by a process limitation. Consequently, absent a showing of an unobvious difference between the claimed product and the prior art, the subject product-by-process claim limitation is not afforded patentable weight (MPEP 2113). The reason for combining is same as claim 1.

Regarding claim 4, Chang discloses the numbers of the conducting lines are 3 each on left and right side of the substrate (501). The reason for combining is same as claim 1.

Regarding claim 5, Chang discloses the conducting lines are made of Al, Cr, or Ag (para 21). The reason for combining is same as claim 1.

Regarding claim 10, Chang discloses a panel for an organic electroluminescent device (figs 2, 3, 5A-5C) comprising:

a substrate (501) having a first conducting area (left portion), a second conducting area (right portion), a third conducting area (bottom portion), a first film (306), and an active area (508);

wherein the active area locates between the first conducting area and the second conducting area; the third conducting area locates at one side of the active area; the first conducting area, the second conducting area, the third conducting area and the active area are integrated together on the surface of the substrate; and the third conducting area locates adjacent to the first conducting area, the second conducting area, and the active area;

first conducting lines (506) located in the first conducting area on the substrate;

second conducting lines (507) located in the second conducting area on the substrate;

third conducting lines (bottom portion of 506 and 507) located in the third conducting area on the substrate;

first electrodes (503) located in the active area, wherein the first electrode connects a third conducting line;

second electrodes (505) located in the active area, wherein the second electrode connects a first conducting line or a second conducting line; and

organic electroluminescent medium (fig 1C, 106) located in the active area, wherein the organic electroluminescent medium is sandwiched between the first electrode (104) and the second electrode (105); and

the first film embedded with fourth conducting lines (not referenced) wherein the fourth conducting lines are electrically connected with the third conducting lines.

The examiner notes in para 26, the bonding unit (502, lateral section) on the substrate (501) is an input end for receiving the output signals to external circuit, hence the third conducting lines which are the conducting lines that transfers signals to cathodes are connected to the fourth conducting lines which are the conducting lines that transfers signals from power source to the cathodes via third conducting lines.

Chang does not disclose the plurality of second electrodes alternate between connecting to a first and a second conducting line.

Yonekura discloses a panel (61) for an organic EL device (fig 9) having a plurality of first electrodes (67) and a plurality of second electrodes (70), and the second electrodes alternate between connecting to a first conducting line (64) and a second conducting line (65), for the purpose of distributing electric current in a balanced manner.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have second electrodes being alternated between connecting a first conducting line and a

second conducting line disclosed by Yonekura in the panel disclosed by Chang, for the purpose of distributing electric current in a balanced manner.

Regarding claim 16, Chang discloses Chang discloses the numbers of the conducting lines are 3 each on left and right side of the substrate (501). The reason for combining is same as claim 10.

Regarding claim 17, Chang discloses the conducting lines are made of Al, Cr, or Ag (para 21). The reason for combining is same as claim 10.

Claims 6-8 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (2003/0193792) in view of Yonekura (2002/0149313), in further view of Lu (6,559,604).

Regarding claim 6, Chang in view of Yonekura discloses all the claimed limitation except for pixel defining layer being located between organic EL medium to define the pixel area of the active area.

Lu discloses an OELD (fig 2) having a pixel defining layer (60) being located between the organic EL medium (30), for the purpose of defining the pixel area.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a pixel defining layer being located between the organic EL medium disclosed by Lu in the panel disclosed by Chang in view of Yonekura, for the purpose of defining the pixel area.

Regarding claim 7, Lu discloses auxiliary electrodes (fig 1, 70) being located on the surface of the first electrodes (20), and the auxiliary electrodes are being used to increase current density of the first electrode. The combining reason is same as claim 6.

Regarding claim 8, Lu discloses isolating walls (col 5, line 53, fig 2, 50) located on the surface of the pixel defining layer (60). The combining reason is same as claim 6.

Regarding claim 18, Chang in view of Yonekura discloses all the claimed limitation except for pixel defining layer being located between organic EL medium to define the pixel area of the active area.

Lu discloses an OELD (fig 2) having a pixel defining layer (60) being located between the organic EL medium (30), for the purpose of defining the pixel area.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a pixel defining layer being located between the organic EL medium disclosed by Lu in the panel disclosed by Chang in view of Yonekura, for the purpose of defining the pixel area.

Regarding claim 19, Lu discloses auxiliary electrodes (fig 1, 70) being located on the surface of the first electrodes (20), and the auxiliary electrodes are being used to increase current density of the first electrode. The combining reason is same as claim 18.

Regarding claim 20, Lu discloses isolating walls (col 5, line 53, fig 2, 50) located on the surface of the pixel defining layer (60). The combining reason is same as claim 18.

Claims 9 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (2003/0193792) in view of Yonekura (2002/0149313), in further view of Ogura (6,924,594).

Regarding claims 9 and 21, Chang in view of Yonekura discloses all the claimed limitation except for a barrier cover located above the active area for preventing the organic EL

medium form the moisture, oxygen, oxide, or sulfide in the air, and the cover is bonded with the panel through sealing.

Ogura discloses an OELD having a barrier cover (fig 1b, 102) being located above the active area (106) for preventing the organic EL medium (105) form the moisture, oxygen, oxide, or sulfide in the air, and the cover is bonded with the panel through sealing (col 3, lines 28-32), for the purpose of increasing the life time of the panel.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a barrier cover located above the active area for preventing the organic EL medium form the moisture, oxygen, oxide, or sulfide in the air, and the cover is bonded with the panel through sealing disclosed by Ogura in the panel disclosed by Chang in view of Yonekura, for the purpose of increasing the life time of the panel.

Claims 11-13 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (2003/0193792) in view of Yonekura (2002/0149313), in further view of Endo (6,507,384).

Regarding claim 11, Chang in view of Yonekura discloses all the claimed limitation except for a PCB, and pins of the integrated circuit being connected with PCB.

Endo discloses a device that can be used as EL device having PCB (fig 9, 3), and pins (12) of IC (10) being connected with PCB, for the purpose of mounting various types electronic parts (col 2, lines 20-22, fig 9) so that the device is functional.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have IC pins connected with PCB disclosed by Endo in the panel disclosed by

Chang in view of Yonekura, for the purpose of mounting various types electronic parts so that the device is functional.

Regarding claim 12, Endo discloses the pins of the IC and the PCB are connected through anisotropic conductive films (col 2, lines 4-26). The reason for combining is same as claim 11.

Regarding claim 13, Endo discloses PCB and a second film (5) wherein part of the pins (14) of the IC connects with the second film, the PCB electrically connects the second film. The reason for combining is same as claim 11.

Regarding claim 22, Endo discloses fifth conductive lines (no shown, however, it would be obvious to have any type of conducting lines in the first film since the purpose of having the first film is to transfer signal from and to controller) embedded in the first film (fig 9, 4) wherein the fourth conducting lines and the fifth conducting lines do not connect to each other directly (power and data signals would not be directly connected to each other), part of pins (12) of the IC electrically connects to the fourth conducting lines, and the other part of pins (10) of the IC electrically connects to the fifth conducting lines. The reason for combining is same as claim 11.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (2003/0193792) in view of Yonekura (2002/0149313), in further view of Holland (4,217,020).

Regarding claim 14, Chang in view of Yonekura discloses all the claimed limitation except for PCB and second film wherein part of pins extends from the IC and is embedded in the second film, and the extended pins embedded in the second film connect to the PCB.

Holland discloses a PCB (fig 2, 26) and a film (34), wherein part of pins (36) extends from IC (20) and is embedded in film (34), and extended pins (36) embedded in film (34) connect to PCB (26), for the purpose of increasing manufacturability.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a PCB and a film, wherein part of pins extends from IC and is embedded in film, and extended pins embedded in film connect to PCB disclosed by Holland in the panel disclosed by Chang in view of Yonekura, for the purpose of increasing manufacturability.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (2003/0193792) in view of Yonekura (2002/0149313), in further view of Holland (4,217,020), in further view of Endo (6,507,384).

Regarding claim 15, Chang in view of Yonekura and Holland discloses all the claimed limitation except for the IC and the PCB being connected through anisotropic conductive films or wire bonding.

Endo discloses the pins of the IC and the PCB are connected through anisotropic conductive films (col 2, lines 4-26), for the purpose of reducing the resistance drop between the IC and PCB.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the pins of the IC and the PCB are connected through anisotropic conductive films disclosed by Endo in the panel disclosed by Chang in view of Yonekura and Holland, for the purpose of reducing the resistance drop between the IC and PCB.

Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (2003/0193792) in view of Yonekura (2002/0149313), in further view of Kawaguchi (5,400,221).

Regarding claim 23, Chang in view of Yonekura discloses all the claimed limitation except for the first film being a hard film for tape carrier package.

Kawaguchi discloses a hard film (col 3, line 47, "PCB", and fig 2A, 12) for tape carrier package (col 3, lines 45-48, fig 2A, 4), for the purpose of having structural ruggedness in the film in order to achieve higher reliability of the panel.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a film made of hard film for TCP disclosed by Kawaguchi in the panel disclosed by Chang in view of Yonekura, for the purpose of having structural ruggedness in the film in order to achieve higher reliability of the panel.

Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (2003/0193792) in view of Yonekura (2002/0149313), in further view of Katsumata (6,826,016).

Regarding claim 24 and 25, Chang in view of Yonekura discloses all the claimed limitation except for electrically passive devices such as capacitors or resistors being bonded on the fourth conducting lines on the first film.

Katsumata discloses film (col 6, lines 44-47, "FBC", fig 14, 52) with capacitors (96) bonded on conducting lines (28), for the purpose of smoothing the power source (col 1, lines 60-63) so that the electrical noise is lessened.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have capacitors being bonded on conducting lines on film disclosed by Katsumata in the panel disclosed by Chang in view of Yonekura, for the purpose of smoothing the power source so that the electrical noise is lessened.

Response to Arguments

Applicant's arguments with respect to claims 1-25 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bumsuk Won whose telephone number is 571-272-2713. The examiner can normally be reached on Monday through Friday, 8:00 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimeshkumar Patel can be reached on 571-272-2457. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Bumsuk Won
Patent Examiner

JOSEPH WILLIAMS
PRIMARY EXAMINER